#9/3-17-04 V. John
A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of HAPKE, FRIEDRICH	Atty. Docket DE 000118
Serial: 09/923,604	Group Art Unit: 2133
Filed: 08/07/2001	Examiner: TRIMMINGS, JOHN P

ARRANGEMENT AND METHOD OF TESTING AN INTEGRATED CIRCUIT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 C.F.R. 1.111

Sir:

Responsive to the Office Action of October 29, 2003, please amend this application as follows:

IN THE CLAIMS

1. (Currently amended) An arrangement for testing an integrated circuit comprising a combinational logic system [(1)] and a test circuit, which arrangement performs a test of the behavior of the combinational logic system [(1)] in comparison with

a1